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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,210	11/12/2003	Walter L. Moden	3725.3US (98-0558.03/US)	6325

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/706,210	MODEN ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- Th MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2003 and 26 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,6,7,9,11,13,15,17,19,21,22,24-26,28,30,31 and 33* is/are rejected.

7)☒ Claim(s) *3,5,8,10,12,14,16,18,20,23,27,29,32 and 34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/12/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 11/12/2003 is acceptable.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1-2, 4, 6-7, 9, 11, 13, 15, 17, 19, 21-22, 24-26, 28, 30-31, and 33** are rejected under 35 U.S.C. 102(e)(2) as being anticipated by Senba et al. U.S. Patent 6,188,127 (the '127 patent, cited by Applicant).

The '127 patent discloses in respective portions of the specification, in Figures 6-7 a stackable assembly, and in Figure 3C a stackable assembly on a substrate, as claimed.

Referring to **claims 1, 6, 11, 15, 25, and 30**, the '127 patent discloses a stackable semiconductor device assembly comprising:

a first carrier 2 having a cavity 21 therein, an upper surface, a lower surface, at least one aperture 5' extending therethrough, and a plurality of circuits (no number) located in a portion of the cavity extending to the at least one aperture;

a semiconductor device 1 having an active surface having a plurality of bond pads 4 thereon, the semiconductor device located within the cavity of the first carrier;

a first connector between at least one circuit of the plurality of circuits located in the portion of the cavity of the first carrier and at least one bond pad of the plurality of bond pads on the active surface of the semiconductor device (column 6, lines 23-25);

encapsulant material 6 filling the portion of the cavity in the first carrier; and

connector material located in the at least one aperture in the first carrier (column 6, lines 28-30).

Referring to **claims 2, 7, 11, 15, 25-26, and 30-31**, although the '127 patent does not explicitly disclose that the stackable semiconductor device assembly of the embodiment of Figures 6-7 further comprises a substrate 12 as in the embodiment of Figures 3, in application the stackable semiconductor device assembly of the embodiment of Figures 6-7 further comprises a substrate 12 as in the embodiment of Figures 3. In other words, in application, the stackable semiconductor device assembly of the embodiment of Figures 6-7 further comprises:

a substrate 12 having an upper surface, a lower surface, and a plurality of circuits (not shown) on the upper surface thereof; and

at least one inherent second connector connected to the connector material in the at least one aperture in the first carrier and at least one circuit of the plurality of circuits on the upper surface of the substrate.

Referring to **claims 4, 9, 13, 17, 28, and 33** , the '127 patent discloses, with reference now back to Figures 6-7, a stackable semiconductor device assembly comprising:

a second carrier oriented with respect to the first carrier and positioned in the same direction as the first carrier and further having a cavity therein, an upper surface, a lower surface, at least one aperture therethrough, and a plurality of circuits located in a portion of the cavity thereon connected to the at least one aperture therethrough;

a second semiconductor device having an active surface having a plurality of bond pads thereon, the second semiconductor device located within the cavity of the second carrier;

another first connector between at least one circuit of the plurality of circuits located in the portion of the cavity of the second carrier and at least one bond pad of the plurality of bond pads on the active surface of the second semiconductor device located in the cavity of the second carrier;

encapsulant material filling the portion of the cavity in the second carrier; and

connector material located in the at least one aperture in the second carrier connected to the connector material in the at least one aperture in the first carrier.

Regarding **claims 19 and 22**, the '127 discloses in the embodiment of Figures 6-7 a stackable semiconductor device assembly that could be used in a substrate 12 of the embodiment of Figure 3C, although which substrate is not explicitly disclosed in the embodiment of Figures 6-7, the stackable semiconductor device assembly comprising:

a substrate 12 having an upper surface, a lower surface, and a plurality of circuits (not shown) on the upper surface thereof;

a first carrier 2 having a cavity 21 therein, an upper surface, a lower surface, at least one aperture 5' extending therethrough, and a plurality of circuits (no number) located in a portion of the cavity extending to the at least one aperture;

a first semiconductor device 1 having an active surface having a plurality of bond pads 4 thereon, the first semiconductor device located within the cavity of the first carrier;

a first connector between at least one circuit of the plurality of circuits located in the portion of the cavity of the first carrier and at least one bond pad of the plurality of bond pads on the active surface of the first semiconductor device (column 6, lines 23-25);

encapsulant material 6 filling the portion of the cavity in the first carrier;

a first connector material located in the at least one aperture in the first carrier (column 6, lines 28-30).

at least one inherent second connector connected to the first connector material in the at least one aperture in the first carrier and at least one circuit of the plurality of circuits on the upper surface of the substrate.

a second carrier 2 oriented with respect to the first carrier and positioned in the same direction as the first carrier and further having a cavity therein, an upper surface, a lower surface, a plurality of connection pads (not shown) on the upper surface thereof, a plurality of connection pads (not shown) on the lower surface thereof, at least one first circuit of a plurality of first circuits connecting at least one connection pad of the plurality of connection pads on the upper surface thereof to at least one connection pad of the plurality of connections pads on the lower surface thereof (column 6, lines 28-30: "the carriers are stacked together and connected by metal, conductive resin or the like via the end through holds 5' "), and at least one second circuit of a

plurality of second circuits located in a portion of the cavity therein connected to the at least one connection pad of the plurality of connection pads on the upper surface thereof and the at least one connection pad of the plurality of connection pads on the lower surface (column 6, lines 23-25: "the electrodes of the chip 1 and those of the carrier 2 are electrically connected", hence there must be at least one second circuit of a plurality of second circuits located in a portion of the cavity connected to the at least one connection pad of the plurality of connection pads on the upper surface and the at least one connection pad of the plurality of connection pads on the lower surface);

a second semiconductor device having an active surface having a plurality of bond pads thereon, the second semiconductor device located within the cavity of the second carrier;

a third connector between the at least one second circuit of a plurality of second circuits located in the portion of the cavity of the second carrier and at least one bond pad of the plurality of bond pads on the active surface of the second semiconductor device;

encapsulant material filling the portion of the cavity in the second carrier; and

at least one fourth connector connected to the at least one connection pad of the plurality of connection pads on the lower surface of the second carrier and at least one circuit of a plurality of circuits on the lower surface of the substrate.

Referring to **claims 21 and 24**, the '127 patent further discloses, in a similar manner for the second carrier:

a third carrier oriented with respect to the first carrier and positioned in the same direction as the first carrier further having a cavity therein, an upper surface, a lower surface, a plurality of connection pads on the upper surface thereof, a plurality of connection pads on the

lower surface thereof, at least one first circuit of a plurality of first circuits connecting at least one connection pad of the plurality of connection pads on the upper surface thereof to at least one connection pad of a plurality of connection pads on the lower surface thereof, and at least one second circuit of a plurality of second circuits located in a portion of the cavity therein connected to the at least one connection pad of the plurality of connection pads on the upper surface thereof and the at least one connection pad of the plurality of connection pads on the lower surface thereof;

a third semiconductor device having an active surface having a plurality of bond pads thereon, the third semiconductor device located within the cavity of the third carrier;

a fifth connector between at least one second circuit of the plurality of second circuits located in a portion of the cavity of the third carrier and the at least one bond pad of the plurality of bond pads on the active surface of the third semiconductor device; and

encapsulant material filling the portion of the cavity in the third carrier.

Allowable Subject Matter

3. **Claims 3, 5, 8, 10, 12, 14, 16, 18, 20, 23, 27, 29, 32, and 34** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a stackable assembly having all exclusive limitations as recited in the above mentioned

claims and their respective independent claims, characterized in that the first carrier includes at least one fin or lip on a portion thereof.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

TH

Tu-Tu Ho
April 26, 2004

David Nelms
Supervisory Patent Examiner
Technology Center 2800